Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original): A high speed and low power sense amplifier circuit comprising:

a precharge circuit, which interfaces with a sense-enable circuit, a sense output circuit, and control logic circuitry,

a sense enable circuit, which interfaces with said precharge circuit, said sense output circuit, and said control logic circuitry,

a sense output circuit, which interfaces with memory cell bit lines, said precharge circuit, said sense enable circuit, and said control logic circuitry, and control logic circuitry.

2. (Original): The high speed and low power sense amplifier circuit of claim 1 wherein said precharge circuit is made up of two n-channel metal-oxide semiconductor field effect transistors, NMOS FETs, and one p-channel metal-oxide semiconductor field effect transistor, PMOS FET.

3. (Original): The high speed and low power sense amplifier circuit of claim 1 wherein said sense enable circuit is made up of three NMOS FETS.

4. (Original): The high speed and low power sense amplifier circuit of claim 1 wherein said sense output circuit consists of three serially connected inverters.

5. (Original): The high speed and low power sense amplifier circuit of claim 1 wherein said control circuitry consists of three inverters and two NOR circuits.

6. (Currently Amended): The high speed and low power sense amplifier circuit of claim 1 wherein said control circuitry has two primary inputs~~:~~, a sense enable signal, and a sense output signal.

7. (Currently Amended): The high speed and low power sense amplifier circuit of claim 1 wherein said control circuitry has two primary outputs~~:~~, an inverted sense enable signal, and a latched precharge signal.

8. (Currently Amended): The high speed and low power sense amplifier circuit of claim 1 wherein said precharge circuit has ~~three~~ two inputs~~:~~, a precharge signal and a sense enable signal.

9. (Original): The high speed and low power sense amplifier circuit of claim 1 wherein said precharge circuit has an output, the precharge signal, Vs.

10. (Currently Amended): The high speed and low power sense amplifier circuit of claim 1 wherein said sense enable circuit has three inputs~~:~~, a sense enable signal and its inverse, and a word line signal.

11. (Original): The high speed and low power sense amplifier circuit of claim 1 wherein said sense enable circuit has an output, a data line.

12. (Original): The high speed and low power sense amplifier circuit of claim 1 wherein said sense output circuit has a sense input and a sense output.

13. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 2 wherein said first NMOS FET in said precharge circuit has its gate attached to said precharge

signal its drain connected to a positive power supply and its source connected to the drain of a second NMOS ~~device~~ FET in said precharge circuit.

14. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 13 wherein said second NMOS FET in said precharge circuit has its gate attached to said sense enable signal, its drain connected to said source of said first NMOS FET of said precharge circuit and its source connected to a node, which feeds the input of said sense output circuit and which feeds the drain of a first NMOS device in said sense enable circuit.

15. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 14 wherein said ~~first~~ PMOS FET in said precharge circuit has its source attached to said Vdd power supply, its gate attached to said precharge signal and its drain connected to said node, which feeds said sense output circuit.

16. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 2 wherein ~~said~~ a first NMOS FET in said sense enable circuit has its drain connected to said source of ~~said~~ a second one of the NMOS FETs of said precharge circuit, its source connected to a data line of a memory ~~away~~ array, and its gate connected to a sense enable signal.

17. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 16 wherein said second NMOS FET of said sense enable circuit has its drain connected to said data line of said memory array, its gate connected to a word line and its source connected to ground.

18. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 14 wherein an ~~third~~ NMOS FET of said sense enable circuit has its drain connected to said node,

which is said input to said sense output circuit, its source is connected to ground, and its gate is connected to an inverse of said sense enable signal.

19. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 7 wherein said sense enable signal feeds an inverter in said control logic to produce said inverted sense enable signal.

20. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 7 wherein said precharge signal comes from a latch circuit within said control circuit.

21. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 20 wherein said latch in said control circuit consists of two 2-input NORs, each having an ~~whose~~ outputs that feeds an input of the other NOR~~s inputs~~.

22. (Original): The high speed and low power sense amplifier circuit of claim 1 wherein a sense enable signal in said control circuit feeds an inverter to produce an inverted sense enable signal, which feeds a first 2-input NOR circuit.

23. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 22, wherein a sense output signal in said control circuit feeds an inverter to produce an inverted sense output signal, which feeds a second 2-input NOR circuit.

24. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 23, wherein one of said 2-input NORs has said inverted sense enable signal as an input.

25. (Currently Amended): The high speed and low power sense amplifier circuit of claim ~~1~~ 24, wherein the other said 2-input NOR circuit has said inverted sense output signal as an input.

26. (Original): A method of developing a high speed and low power sense amplifier circuit comprising the steps:

providing a precharge circuit, which interfaces with a sense-enable circuit, a sense output circuit, and control logic circuitry,

providing a sense enable circuit, which interfaces with said precharge circuit, said sense output circuit, and said control logic circuitry,

providing a sense output circuit, which interfaces with memory cell bit lines, said precharge circuit, said sense enable circuit, and said control logic circuitry, and

providing control logic circuitry.

27. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said precharge circuit is made up of two n-channel metal-oxide semiconductor field effect transistors, NMOS FETs, and one p-channel metal-oxide semiconductor field effect transistor, PMOS FET.

28. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said sense enable circuit is made up of three NMOS FETS.

29. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said sense output circuit consists of three serially connected inverters.

30. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said control circuitry consists of three inverters and two NOR circuits.

31. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said control circuitry has two primary inputs;~~, a precharge signal,~~ a sense enable signal, and a sense output signal.

32. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said control circuitry has two primary outputs;~~,~~ an inverted sense enable signal, and a latched precharge signal.

33. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said precharge circuit has two inputs;~~,~~ a precharge signal and a sense enable signal.

34. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 33, wherein said precharge circuit has an output;~~,~~ the precharge signal, Vs.

35. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said sense enable circuit has three inputs;~~,~~ a sense enable signal and its inverse, and a word line signal.

36. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said sense enable circuit has a data line as an output~~, a data line~~.

37. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein said sense output circuit has a sense input and a sense output.

38. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim 27 wherein ~~said~~ a first one of the NMOS FETs in said precharge circuit has its gate ~~attached to said~~ connected to receive a precharge signal, its drain connected to a positive power supply and its source connected to the drain of a second one of the NMOS ~~device~~ FETs in said precharge circuit.

39. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 38, wherein said second NMOS FET in said precharge circuit has its gate attached to said sense enable signal, its drain connected to said source of said first NMOS FET of said precharge circuit and its source connected to a node, which feeds the input of said sense output circuit and which feeds the drain of a first NMOS device in said sense enable circuit.

40. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 39, wherein said first PMOS FET in said precharge circuit has its source attached to ~~said~~ a Vdd power supply, its gate attached to said precharge signal and its drain connected to said node, which feeds said sense output circuit.

41. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim 27 wherein ~~said~~ a first NMOS FET in said sense enable circuit has its drain connected to ~~said~~ a source of said second NMOS FET of said precharge circuit its source connected to a data line of a memory ~~away~~ array, and its gate connected to receive a sense enable signal.

42. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 41, wherein ~~said~~ a second NMOS FET of said sense enable circuit has its drain connected to said data line of said memory array, its gate connected to a word line and its source connected to ground.

43. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 42, wherein a third NMOS FET of said sense enable circuit has its drain connected to said node, which is said input to said sense output circuit, its source ~~is~~ connected to ground and its gate is connected to an inverse of said sense enable signal.

44. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 41, wherein said sense enable signal feeds an inverter in said control logic to produce said inverted sense enable signal.

45. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 31, wherein said precharge signal comes from a latch circuit within said control circuit.

46. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 45, wherein said latch in said control circuit consists of two 2-input NORs whose outputs feed the other NORs inputs.

47. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 26, wherein a sense enable signal in said control circuit feeds an inverter to produce an inverted sense enable signal, which feeds a first 2-input NOR circuit.

48. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 47, wherein a sense output signal in said control circuit feeds an inverter to produce an inverted sense output signal, which feeds a second 2-input NOR circuit.

49. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 48, wherein one of said 2-input NORs has said inverted sense enable signal as an input.

50. (Currently Amended): The method of developing a high speed and low power sense amplifier circuit of claim ~~27~~ 49, wherein the other said 2-input NOR circuit has said inverted sense output signal as an input.